SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-180374; filed September 14, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

It is expected that silicon carbide (SiC) is used for a material for a next-generation semiconductor device. SiC has characteristics in which the magnitude of bandgap is approximately three times, breakdown field strength is approximately 10 times, and thermal conductivity is approximately three times, compared to silicon (Si). For this reason, it is possible to realize a semiconductor device which has low loss and can perform a high temperature operation by using SiC.

A semiconductor device which uses SiC has a problem in which reliability decreases due to delamination of an electrode film.

An example of related art includes Japanese Patent No. 3871607.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view of a semiconductor device according to a first embodiment.

FIG. 2 is a flowchart of a fabrication method of the semiconductor device according to the first embodiment.

FIG. 3 is a schematic sectional view of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the first embodiment.

FIG. 4 is a schematic sectional view of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the first embodiment.

FIG. 5 is a schematic sectional view of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the first embodiment.

FIG. 6 is a schematic sectional view of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the first embodiment.

FIG. 7 is a schematic sectional view of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the first embodiment.

FIG. 8 is a schematic sectional view of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the first embodiment.

FIG. 9 is a schematic sectional view of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the first embodiment.

FIGS. 10A to 10D are views illustrating actions and effects of the first embodiment.

FIG. 11 is a schematic sectional view of a semiconductor device according to a second embodiment.

FIG. 12 is a schematic sectional view of the semiconductor device in the process of fabrication according to a fabrication method of the semiconductor device according to the second embodiment.

FIG. 13 is a schematic sectional view of a semiconductor device according to a third embodiment.

FIG. 14 is a schematic sectional view of a semiconductor device according to a fourth embodiment.

DETAILED DESCRIPTION

[0005]Exemplary embodiments provide a semiconductor device which prevents reliability from decreasing due to delamination of an electrode film.

[0006]In general, according to one embodiment, there is provided a semiconductor device including a silicon carbide layer which includes a first surface, and a second surface that is provided on a side opposite to the first surface; a first insulating film which is provided on the first surface; a first electrode which is provided on the first insulating film; a first silicon carbide region of a first conductive type which is provided in the silicon carbide layer and a part of which is provided on the first surface; a second silicon carbide region of a second conductive type which is provided in the first silicon carbide region, and a part of which is provided on the first surface; a third silicon carbide region of a first conductive type which is provided in the second silicon carbide region, and a part of which is provided on the first surface; a second electrode which is provided on the second surface and contains a metal, silicon, and carbon; and a third electrode which is provided so as to come into contact with the third silicon carbide region, contains the metal, the silicon, and the carbon, and whose carbon concentration is higher than carbon concentration of the second electrode.

[0008]Hereinafter, embodiments of the invention will be described with reference to the drawings.

[0009]In the present specification, the same symbols or reference numerals will be attached to the same or similar members, and repeated description thereof will be omitted.

[0010]Hereinafter, a case in which a first conductive type is an n-type and a second conductive type is a p-type will be used as an example. In addition, in the present specification, notation of n+, n and n-, and p+, p and p- represents relative levels of impurity concentrations of each conductive type. That is, it represents that n+-type impurity concentration is relatively higher than n-type impurity concentration, and n--type impurity concentration is relatively lower than n-type impurity concentration. In addition, it represents that p+-type impurity concentration is relatively higher than p-type impurity concentration, and p--type impurity concentration is relatively lower than p-type impurity concentration. There is a case in which n+ and n- are simply described as an n type, and p+ and p- are simply described as a p type.

[0011]In the specification, in order to represent a positional relationship of components or the like, an upward direction of the drawing is referred to as “upper”, and a downward direction of the drawing is referred to as “lower”. In the specification, concept of “upper” and “lower” may not be necessarily the terms representing a relationship between directions of gravity.

[0012]In the specification, a case in which “A and B are provided so as to come into contact with each other” involves a case in which A and B come into direct contact with each other, and a case in which A and B are provided so as to come into indirect contact with each other through an intermediate layer or the like provided between A and B.

First Embodiment

[0013]A semiconductor device according to the present embodiment includes a silicon carbide layer which includes a first surface, and a second surface that is provided on a side opposite to the first surface; a first insulating film which is provided on the first surface; a first electrode which is provided on the first insulating film; a first silicon carbide region of a first conductive type which is provided in the silicon carbide layer and a part of which is provided on the first surface; a second silicon carbide region of a second conductive type which is provided in the first silicon carbide region, and a part of which is provided on the first surface; a third silicon carbide region of a first conductive type which is provided in the second silicon carbide region, and a part of which is provided on the first surface; a second electrode which is provided on the second surface and contains a metal, silicon, and carbon; and a third electrode which is provided so as to come into contact with the third silicon carbide region, contains the metal, the silicon, and the carbon, and whose carbon concentration is higher than carbon concentration of the second electrode.

[0014]FIG. 1 is a schematic sectional view of a semiconductor device according to the present embodiment.

[0015]A semiconductor device 100 includes a silicon carbide layer 10, a first electrode 34, a second electrode 30, a third electrode 32, a first insulating film 40, and a second insulating film 42.

[0016]The silicon carbide layer 10 includes a first surface, and second surface provided on a side opposite to the first surface. The silicon carbide layer 10 includes an n-type drift region (first silicon carbide region) 10b, a p-type well region (second silicon carbide region) 20, an n-type source region (third silicon carbide region) 22, a p-type contact region (fourth silicon carbide region) 24, and an n-type drain region (fifth silicon carbide region) 10a, therein.

[0017]The semiconductor device 100 according to the present embodiment is formed by injecting ions into the well region 20 and the source region 22, and is a double implantation metal oxide semiconductor field effect transistor (DI MOSFET).

[0018]The n-type first silicon carbide layer 10b is provided in the silicon carbide layer 10, and a part thereof is provided on a first surface 14. The first silicon carbide layer 10b functions as a drift region of a MOSFET. The first silicon carbide layer 10b contains, for example, n-type impurity higher than or equal to 5´1015 cm-3 and lower than or equal to 5´1016 cm-3. The impurity concentration of the first silicon carbide layer 10b is lower than impurity concentration of the fifth silicon carbide region 10a which will be described below.

[0019]The first insulating film 40 is provided on the first surface 14. The first insulating film 40 is a gate insulating film. The first insulating film 40 is, for example, a silicon oxide film or a high-k film.

[0020]The first electrode 34 is provided on the first insulating film 40. The first electrode 34 is a gate electrode. The first electrode 34 contains, for example, polycrystalline silicon in which impurity is doped.

[0021]The p-type well region 20 is provided in the first silicon carbide layer 10b, and a part thereof is provided on the first surface 14. The well region 20 functions as a channel region of a MOSFET. A depth of the well region 20 is, for example, approximately 0.6 mm. The well region 20 contains, for example, p-type impurity higher than or equal to 5´1015 cm-3 and lower than or equal to 1´1019 cm-3. The p-type impurity is, for example, aluminum (Al), boron (B), gallium (Ga), or indium (In).

[0022]The n-type source region 22 is provided in the well region 20, and a part thereof is provided on the first surface 14. The source region 22 functions as a source of a MOSFET. A depth of the source region 22 is, for example, approximately 0.3 mm and is smaller than the well region 20. The source region 22 contains, for example, n-type impurity higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1021 cm-3. The n-type impurity is, for example, phosphorus (P), nitride (N), arsenic (As), or antimony (Sb).

[0023]The p-type contact region 24 is provided in the well region 20, and is electrically coupled to the third electrode 32 which will be below. The contact region 24 is used to reduce a contact resistance between the well region 20 and the third electrode 32 which will be described below. A depth of the contact region 24 is, for example, approximately 0.3 mm and is smaller than the well region 20. The contact region 24 contains, for example, p-type impurity higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1021 cm-3. The impurity concentration of the contact region 24 is higher than impurity concentration of the well region 20.

[0024]The second electrode 30 is provided on a second surface 12. The second electrode 30 is a drain electrode. The second electrode 30 includes a first electrode layer 30a which contains a metal and silicon, and a second electrode layer 30b which contains a metal, silicon, and a carbon, and is provided between the first electrode layer 30a the silicon carbide layer 10. A thickness of the first electrode layer 30a is, for example, approximately 500 nm. A thickness of the second electrode layer 30b is, for example, approximately 100 nm.

[0025]It is preferable that the first electrode layer 30a contains metal silicide (compound of metal and silicon). It is preferable that the metal is nickel in order to reduce a contact resistance.

[0026]It is preferable that the second electrode layer 30b includes a first phase 30b1 containing metal silicide and carbon, and a second phase 30b2 containing carbon. It is preferable that the metal is nickel in order to reduce a contact resistance.

[0027]The third electrode 32 is provided in the source region 22 so as to come into contact with the source region 22. The third electrode 32 is electrically coupled to the third silicon carbide region 22 and the fourth silicon carbide region 24. The third electrode 32 is a source electrode. The third electrode 32 contains a metal, silicon, and carbon. Carbon concentration of the third electrode 32 is higher than carbon concentration of the second electrode 30. It is preferable that the third electrode 32 contains metal silicide. It is preferable that the metal is nickel in order to form a good Ohmic contact

[0028]Carbon concentration of the second electrode 30 and carbon concentration of the third electrode 32 can be measured by a transmission electron microscope-energy dispersive X-ray spectroscopy (TEM-EDX). In each of the second electrode 30 and the third electrode 32, carbon concentration of the center in a thickness direction is measured inside a surface in parallel with the thickness direction, and thereby carbon concentration is obtained. Spatial resolution in a case in which the carbon concentration is measured is, for example, 5 nm.

[0029]The fifth silicon carbide region 10a is provided in the silicon carbide layer 10 between the first silicon carbide region 10b and the second electrode 30. The fifth silicon carbide region 10a contains, for example, n-type impurity higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1020 cm-3, and is n-type 4H-SiC. For example, it is preferable that 3C-SiC or 6H-SiC are also used. The n-type impurity is, for example, nitride (N), arsenic (As), phosphorus (P), or antimony (Sb).

[0030]The second insulating film 42 is provided on an upper portion of the first insulating film 40, and on a side and an upper portion of the first electrode 34. The second insulating film 42 electrically decouples the third electrode 32 from the first electrode 34.

[0031]Next, a fabrication method of the semiconductor device 100 according to the present embodiment will be described. FIG. 2 is a flowchart of the fabrication method of the semiconductor device according to the present embodiment. FIGS. 3 to 9 are schematic sectional views of the semiconductor device in the process of fabrication according to the fabrication method of the semiconductor device according to the present embodiment.

[0032]According to the fabrication method of the semiconductor device 100 according to the present embodiment, the first silicon carbide region 10b of an n-type is formed on the fifth silicon carbide region 10a of an n-type, the well region 20 is formed on the first silicon carbide region 10b so as to come into contact with the first surface 14, the source region 22 is formed in the well region 20 so as to come into contact with the first surface 14, the contact region 24 is formed on a side of the source region 22 on the well region 20 so as to come into contact with the first surface 14, the first insulating film 40 is formed on the first surface 14, the first electrode 34 is formed on the first insulating film 40, the second insulating film 42 is formed on the first insulating film 40 and the first electrode 34, a first film 52 is formed on the first silicon carbide region 10b, the well region 20, the source region 22, the contact region 24, the first insulating film 40, and the second insulating film 42, first thermal processing is performed, the first film 52 which does not react is removed, a second film 54 is formed so as to come into contact with the second surface, and second thermal processing is performed.

[0033]First, as illustrated in FIG. 3, the first silicon carbide region 10b of an n-type is formed on the fifth silicon carbide region 10a of an n-type by, for example, an epitaxial method (S10). The fifth silicon carbide region 10a and the first silicon carbide region 10b configure the silicon carbide layer 10. A surface of the first silicon carbide region 10b is the first surface 14, and a surface on a side opposite to the first surface 14 is the second surface 12.

[0034]Subsequently, as illustrated in FIG. 4, the well region 20 is formed on the first silicon carbide region 10b so as to come into contact with the first surface 14, by injecting, for example, Al ion. (S12).

[0035]Subsequently, the source region 22 is formed in the well region 20 so as to come into contact with the first surface 14, by injecting, for example, P ion (S14). In addition, the contact region 24 is formed on a side of the source region 22 on the well region 20 so as to come into contact with the first surface 14 (S16). Thereafter, thermal processing for activating the well region 20, the source region 22, and the contact region 24 is performed.

[0036]Subsequently, as illustrated in FIG. 5, the first insulating film 40 is formed on the first surface 14 by, for example, a thermal oxidation method or chemical vapor deposition (CVD) method (S18). Subsequently, the first electrode 34 containing, for example, polycrystalline silicon is formed on the first insulating film 40, and thereafter etching is performed (S20).

[0037]Subsequently, as illustrate in FIG. 6, the second insulating film 42 containing, for example, silicon oxide film is formed on the first insulating film 40 and the first electrode 34. Subsequently, a part on the source region 22 and a part of the second insulating film 42 formed on the contact region 24 are removed by, for example, etching (S22).

[0038]Subsequently, as illustrated in FIG. 7, the first film 52 containing, for example, nickel (Ni) is formed on the first silicon carbide region 10b, the well region 20, the source region 22, the contact region 24, the first insulating film 40, and the second insulating film 42 (S24).

[0039]Subsequently, first thermal processing is performed. By doing so, the source region 22 and the contact region 24 react with the first film 52, and thereby the third electrode 32 which is a metal semiconductor compound layer containing nickel silicide is formed (S26).

[0040]Subsequently, as illustrated in FIG. 8, the first film 52 which does not react is removed by an acid solution or the like containing sulfuric acid (S28).

[0041]Subsequently, as illustrated in FIG. 9, the second film 54 containing NiSi is formed so as to come into contact with the second surface, by, for example, a sputtering method (S30). It is preferable that a ratio between Ni and Si is between 2:1 and 1:3, in order to reduce a silicide reaction of the fifth silicon carbide region.

[0042]It is preferable that a thickness of the second film 54 is greater than or equal to 100 nm and smaller than or equal to 1000 nm. If the thickness is smaller than 100 nm, reaction with the fifth silicon carbide region 10a which will be described below occurs in the entirety of the second film 54, the amount of the second phase 30b2 being generated is increased, and a contact resistance increases. Meanwhile, if the thickness is greater than 1000 nm, heat which is produced from the semiconductor device 100 cannot be dissipated efficiently from a heatsink or the like provided in a lower portion of the semiconductor device 100.

[0043]Subsequently, second thermal processing is performed, the second electrode 30 is formed by reacting the second film 54 with the fifth silicon carbide region 10a (S32), and thereby the semiconductor device 100 illustrated in FIG. 1 is fabricated.

[0044]For example, the temperature of the second thermal processing is higher than or equal to 800°C and lower than or equal to 1050°C. If the temperature is lower than 800°C, the second film 54 and the fifth silicon carbide region 10a do not sufficiently react with each other due to too low temperature, and thereby the contact resistance increases. Meanwhile, if the temperature is higher than 1050°C, the second phase 30b2 occurs too much due to too high temperature, and delamination of the film of the second electrode 30 easily occurs.

[0045]The second thermal processing is performed in an atmosphere of inert gas such as argon (Ar). In addition, time in which the second thermal processing is performed is, for example, approximately four minutes.

[0046]Subsequently, actions and effects of the semiconductor device 100 according to the present embodiment will be described.

[0047]FIGS. 10A to 10D are views illustrating actions and effects of the present embodiment. FIG. 10A is a schematic sectional view of a second film 55 and the fifth silicon carbide region 10a before the second thermal processing in the semiconductor device which becomes a comparative form of the present embodiment. FIG. 10B is a schematic sectional view of a second electrode 31 and the fifth silicon carbide region 10a after the second thermal processing in the semiconductor device which becomes a comparative form of the present embodiment. FIG. 10C is a schematic sectional view of the second film 54 and the fifth silicon carbide region 10a before the second thermal processing in the semiconductor device 100 according to the present embodiment. FIG. 10D is a schematic sectional view of the second electrode 30 and the fifth silicon carbide region 10a after the second thermal processing in the semiconductor device 100 according to the present embodiment.

[0048]In FIG. 10A, nickel (Ni) is used for the second film 55. In this case, as illustrated in FIG. 10B, the entirety of the second film 55 reacts with the fifth silicon carbide region 10a by the second thermal processing. In the second electrode 31 formed by doing so, carbon (C) is diffused in Ni, and thus the entirety of the second electrode 31 becomes the first phase 31b1 which contains Ni and C. In other words, an electrode layer corresponding to the first electrode layer 30a in the semiconductor device 100 illustrated in FIG. 1 is not provided. In addition, on a side, which is close to the fifth silicon carbide region 10a, of the second electrode 31, lots of second phases 31b2 which are formed of carbon (C) are provided. The second phase 31b2 causes a film of the second electrode to be delaminated.

[0049]In FIG. 10C, NiSi is used for the second film 54. In this case, as illustrated in FIG. 10D, after the second thermal processing, a first electrode layer 30a with small amount of contained carbon, and a second electrode layer 30b including the first phase 30b1 and the second phase 30b2 which are provided between the first electrode layer 30a and the fifth silicon carbide region 10a, are formed. If the second film 54 contains Si, the amount of the fifth silicon carbide region 10a which reacts with the second film 54 decreases. For this reason, the amount of the second phase 30b2 which is formed in the second electrode 30 is small. Hence, the film of the second electrode 30 is prevented from being delaminated.

[0050]In order to form the third electrode 32, the first film 52 which does not react is removed by an acid solution containing sulfuric acid, and thereby the third electrode 32 can be simply formed. Accordingly, it is possible to use a metal film which does not contain silicon, for example, a film which does not contain nickel as the first film 52. In this case, the amount of reaction of the source region 22 and the contact region 24 which react with the first electrode 52 decreases, and thus the carbon concentration of the third electrode becomes higher than the carbon concentration of the second electrode. In this case, it is preferable that the carbon concentration of the third electrode is higher than or equal to 1´1018 atoms/cm3.

[0051]In addition, a thickness of the second electrode 30 is greater than a thickness of the third electrode 32, but it is preferable that film delamination is prevented by increasing strength of the second electrode 30 and a contact resistance of the third electrode 32 is reduced.

[0052]As such, according to the semiconductor device 100 according to the present embodiment, it is possible to provide a semiconductor device which prevents reliability from decreasing due to film delamination of the second electrode (drain electrode).

Second Embodiment

[0053]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that a fourth electrode 35 containing meal silicide functions as a gate electrode. Here, description of the contents which overlap those of the first embodiment will be omitted.

[0054]FIG. 11 is a schematic sectional view of the semiconductor device according to the present embodiment.

[0055]In the semiconductor device according to the present embodiment, the fourth electrode 35 is provided on the first insulating film 40. The second insulating film 42 is provided on a side of the fourth electrode 35 on the first insulating film 40. In addition, a third insulating film 44 is provided on the second insulating film 42 and the fourth electrode 35.

[0056]FIG. 12 is a schematic sectional view of the semiconductor device in the process of fabrication according to a fabrication method of the semiconductor device according to the present embodiment. In the fabrication method of the semiconductor device according to the present embodiment, the first film 52 is formed on a silicon film 50 formed of polycrystalline silicon, the source region 22, and the contact region 24. Thereafter, first thermal processing is performed, the silicon film 50 and the first film 52 react with each other, and thereby the fourth electrode 35 which is a layer of metal semiconductor compound containing nickel silicide is formed. In addition, the first film 52 which does not react is removed by an acid solution containing sulfuric acid, and thereafter the third insulating film 44 is formed on the second insulating film 42 and the fourth electrode 35. Others except for these points are the same as the fabrication method of the semiconductor device according to the first embodiment.

[0057]In a case of a gate electrode which uses polycrystalline silicon, an interface depletion layer is formed. Meanwhile, in the semiconductor device 200 according to the present embodiment, metal silicide is used for the gate electrode, and thus the interface depletion layer is not formed. For this reason, according to the semiconductor device 200 according to the present embodiment, it is possible to provide a semiconductor device which is more appropriate for a high frequency operation.

Third Embodiment

[0058]A semiconductor device according to the present embodiment is different from the semiconductor devices according to the first and second embodiments in that a sixth silicon carbide region 10c of a p+-type is provided instead of the n-type drain region (fifth silicon carbide region) 10a. Here, description of the contents which overlap those of the first and second embodiments will be omitted.

[0059]FIG. 13 is a schematic sectional view of the semiconductor device according to the present embodiment.

[0060]In the semiconductor device 300 according to the present embodiment, the sixth silicon carbide region 10c is a silicon carbide layer of p+-type. The sixth silicon carbide region 10c contains aluminum (Al) with impurity concentration, for example, higher than or equal to 1´1018 atoms/cm3 and lower than or equal to 1´1020 atoms/cm3, as p type impurity. The sixth silicon carbide region 10c functions as a collector region of the semiconductor device 300. The semiconductor device 300 according to the present embodiment is an insulated gate bipolar transistor (IGBT).

[0061]The second electrode 30 functions as a collector electrode. In addition, the third electrode 32 functions as an emitter electrode.

[0062]According to the semiconductor device 300 according to the present embodiment, it is possible to provide a semiconductor device which prevents reliability from decreasing due to film delamination of the second electrode (collector electrode).

Fourth Embodiment

[0063]A semiconductor device according to the present embodiment includes a silicon carbide layer which includes a first surface, and a second surface that is provided on a side opposite to the first surface; a first silicon carbide region of a first conductive type which is provided in the silicon carbide layer; a second silicon carbide region of a second conductive type which is provided in the silicon carbide layer on the first silicon carbide region, and a part of which is provided on the first surface; a first electrode which is provided on the first surface and contains a metal, silicon, and carbon; a second electrode which is provided on the second surface, contains the metal, the silicon, and the carbon, and whose carbon concentration is lower than carbon concentration of the first electrode; and a third silicon carbide region of a first conductive type which is provided in the silicon carbide layer between the first silicon carbide region and the second electrode, and a part of which is provided on the second surface. The semiconductor device according to the present embodiment is a PIN type diode. Here, description of the contents which overlap those of the first to third embodiments will be omitted.

[0064]FIG. 14 is a schematic sectional view of the semiconductor device according to the present embodiment.

[0065]The third electrode 32 according to the first to third embodiments corresponds to the first electrode 34 according to the present embodiment. The second electrode 30 functions as a cathode electrode, and the first electrode 34 functions as an anode electrode. A third silicon carbide region 10d functions as an n-type emitter layer, the first silicon carbide region 10b functions as an n--type base layer, and a fourth silicon carbide layer 18 functions as a p-type emitter layer.

[0066]According to the semiconductor device according to the present embodiment, it is possible to provide a semiconductor device which prevents reliability from decreasing due to film delamination of the second electrode (cathode electrode).

[0067]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a silicon carbide layer which includes a first surface, and a second surface that is provided on a side opposite to the first surface;

a first insulating film which is provided on the first surface;

a first electrode which is provided on the first insulating film;

a first silicon carbide region of a first conductive type which is provided in the silicon carbide layer and a part of which is provided on the first surface;

a second silicon carbide region of a second conductive type which is provided in the first silicon carbide region, and a part of which is provided on the first surface;

a third silicon carbide region of a first conductive type which is provided in the second silicon carbide region, and a part of which is provided on the first surface;

a second electrode which is provided on the second surface and contains a metal, silicon, and carbon; and

a third electrode which is provided so as to come into contact with the third silicon carbide region, contains the metal, the silicon, and the carbon, and whose carbon concentration is higher than carbon concentration of the second electrode.

2. The device according to Claim 1, wherein the carbon concentration of the third electrode is higher than or equal to 1´1018 atoms/cm3.

3. The device according to Claim 1 or 2, wherein a thickness of the second electrode is greater than a thickness of the third electrode.

4. The device according to any one of Claims 1 to 3, wherein the second electrode includes

a first electrode layer which contains the metal and the silicon; and

a second electrode layer which contains the metal, the silicon, and the carbon, and is provided between the first electrode layer and the silicon carbide layer.

5. The device according to any one of Claims 1 to 4, wherein the metal is nickel.

6. The device according to any one of Claims 1 to 5, further comprising:

a fourth silicon carbide region of a second conductive type which is provided in the second silicon carbide region, is electrically coupled to the third electrode, and whose impurity concentration is higher than impurity concentration of the second silicon carbide region.

7. The device according to any one of Claims 1 to 6, further comprising:

a fifth silicon carbide region of a first conductive type which is provided in the silicon carbide layer between the first silicon carbide region and the second electrode.

8. The device according to any one of Claims 1 to 6, further comprising:

a sixth silicon carbide region of a second conductive type which is provide in the silicon carbide layer between the first silicon carbide region and the second electrode.

9. A semiconductor device comprising:

a silicon carbide layer which includes a first surface, and a second surface that is provided on a side opposite to the first surface;

a first silicon carbide region of a first conductive type which is provided in the silicon carbide layer;

a second silicon carbide region of a second conductive type which is provided in the silicon carbide layer on the first silicon carbide region, and a part of which is provided on the first surface;

a first electrode which is provided on the first surface and contains a metal, silicon, and carbon;

a second electrode which is provided on the second surface, contains the metal, the silicon, and the carbon, and whose carbon concentration is lower than carbon concentration of the first electrode; and

a third silicon carbide region of a first conductive type which is provided in the silicon carbide layer between the first silicon carbide region and the second electrode, and a part of which is provided on the second surface.

ABSTRACT

According to one embodiment, a semiconductor device includes a silicon carbide layer which includes a first surface, and a second surface that is provided on a side opposite to the first surface; a first insulating film which is provided on the first surface; a first electrode which is provided on the first insulating film; a first silicon carbide region of a first conductive type which is provided in the silicon carbide layer and a part of which is provided on the first surface; a second silicon carbide region of a second conductive type which is provided in the first silicon carbide region, and a part of which is provided on the first surface; a third silicon carbide region of a first conductive type which is provided in the second silicon carbide region, and a part of which is provided on the first surface; a second electrode which is provided on the second surface and contains a metal, silicon, and carbon; and a third electrode which is provided so as to come into contact with the third silicon carbide region, contains the metal, the silicon, and the carbon, and whose carbon concentration is higher than carbon concentration of the second electrode.

DRAWINGS

FIG. 2

START

S10: FORM FIRST SILICON CARBIDE REGION

S12: FORM WELL REGION

S14: FORM SOURCE REGION

S16: FORM CONTACT REGION

S18: FORM FIRST INSULATING FILM

S20: FORM SILICON FILM

S22: FORM SECOND INSULATING FILM

S24: FORM FIRST FILM

S26: PERFORM FIRST THERMAL PROCESSING AND FORM THIRD ELECTRODE

S28: REMOVE FIRST FILM WHICH DOES NOT REACT

S30: FORM SECOND FILM

S32: PERFORM SECOND THERMAL PROCESSING AND FORM FIRST ELECTRODE

END